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Solution of Power Flow and Outage Problems Using Diakoptics and Compensation

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ABSTRACT. The paper describes a diakoptical technique for power flow solution of very large size power systems and combines both diakoptics and compensation methods for simulating branch outages without reconstructing or refactorizing the system matrices of the preoutage state. The proposed technique can either be used in a single-processor computer for sequential solution of torn subdivisions or in a multi-computer configuration (group of single-processor computers or a multiple-processor computer) for a faster solution by parallel processing of torn subdivisions. It can be used for both off- and on-line applications and can use either the bus impedance matrix or the factorized bus admittance matrix of torn subdivisions.

The proposed technique produces exactly the same power flow solution and retains the convergence property of the original untorn system. As compared with the full power flow solution of outage problems, the proposed technique provides very accurate results of post-contingent system voltages (magnitude and angle) and line power flows (active and reactive) for single and multiple outage studies in a faster and most economical way.

Included in this paper are procedures for single and parallel processing solution schemes and test results.

1. Introduction

In power flow methods, the solution time and storage requirements vary with the number of buses in the system under study. These obvious practical limitations have restricted the applications of these methods for very large size networks. Over the last 30 years, a number of publications have appeared involving diakoptical or piecewise solution techniques of the power flow problem of very large size power systems[1-5]. A large system was torn into subdivisions (areas). Each subdivision is handled independently for the partial solution of the problem. Solutions of subdivisions are later modified to account for tearing and finally the modified solutions are combined to provide the solution for the untorn system.

Diakoptic formulation is characterized by its resulting block-diagonal-form matrix structure which is suitable for parallel processing. Diakoptical techniques do not appear to provide savings in time if performed on a single processor in a sequential mode. However, there is a great potential for these techniques for perform well in the multicomputer configuration or in the multiprocessor environment using parallel processing which allows the solution of the problem such as the torn areas to be carried out simultaneously, either in a multiprocessor computer or in a multiplicity of computers.

This paper describes a diakoptical technique for power flow solution of very large size power systems by using either the explicit impedance-bus matrix or the factorized admittance-bus matrix. The subject matter of the paper is considered to be of great importance and very timely since processors costs are coming down and dedicated multiprocessor systems are emerging. The solution procedure is conceptually simple and easy to implement. The results obtained are exact and convergence characteristics are identical to the system solved as a whole. Execution of the parallel solution of the power flow problem using the proposed diakoptical technique is demonstrated in this paper.

The use of full power flow solution methods for outage (contingency) studies provides excellent accuracy but is expensive computationally and excessively demanding of engineering time. Since the need is generally for identification of acceptable or unacceptable outage cases, economy and speed of calculations for the process of identification are of paramount importance. An absolute accuracy in calculations is of secondary importance as the results within engineering tolerances are generally sufficient[6-14].

This paper shows that the diakoptical technique proposed for the power flow solution is combined with compensation[15] to simulate the outage of a network element without refactorizing the base case matrices and starting from the base case power flow. The proposed technique determines post contingent network voltages and power flows should the contingency occur, fast and in a most economical way. The proposed technique provides accurate results and is faster and the full power flow solution. It can be used for single and multiple contingencies.

As compared to other known techniques[6-7] the proposed technique does not make any approximations and removal of shunt elements associated with the outaged branches is correctly simulated in the contingency calculations.

Included in this paper are results of the application of the proposed technique for power flow and contingency studies of a sample system.

2. Development of Proposed Technique

The diakoptical technique of Reference [5] for power flow solution of very large-size power systems using the bus-admittance matrix is taken as the starting step for the development of the proposed technique. It has been modified to include the following additional features :

a) It can be used for parallel processing (solution) using either a multiprocessor computer or a multiplicity of computers. Either the Z-bus matrix or the factorized Y-bus matrix can be used in the proposed technique.

b) It can be used for fast and accurate solution of outages (contingencies) problems using compensation methods[15].

In the proposed technique, shunt elements such as shunt capacitors and reactors, and line charging capacitance are not included in the construction of the admittance – matrix of the torn subdivisions and instead are grouped as shunt admittances at their corresponding buses. This method of representation of shunt elements leads to more accurate simulation of the removal of outaged branches compared to other methods[6,16] in which these elements are kept unchanged in the outaged state matrices.

2.1 Basic Formulation of Power Flow Problem

The basic analytical formulation of the power flow problem is well known[17,18] and is therefore presented briefly in this section.

The total current at bus p of an n-bus system is

$$I_p = (P_p - j\, Q_p) \;/\; E_p^* - y_p\, E_p \qquad p = 1, 2, \cdots, n \qquad p + s \text{ (slack)} \tag{1}$$

where y_p is the total shunt admittance at the bus and $y_p\ E_p$ is the shunt current flowing from bus p to ground. P_p and Q_p are net bus injected active and reactive powers and E_p is bus complex voltage. In this case shunt elements to ground are not included in the parameter matrix.

Selecting a flat voltage start, bus currents can be calculated from Equation (1) above. A new estimate of voltages can be obtained, then, from the following matrix equation

$$E = Y^{-1}\, I + E_s \quad \text{or} \quad E = Z\, I + E_s \tag{2}$$

where Z ($= Y^{-1}$, inverse of bus-admittance matrix) is formed by using the slack bus (s) as reference and E_s is a vector whose elements are all equal to the voltage of the slack bus (dimensions $n - 1 * n - 1$).

The simultaneous-displacement mode (Gauss-Jacobi)[4] of the Z matrix method is used in the proposed technique where the sparse triangular factors of Y-matrix can be used instead of Z, with a great saving in storage and computation per iteration. The new voltage estimates are used in Equation (1) to recalculate bus currents. The process is repeated until changes in all bus voltages are within a specified tolerance.

2.2 Construction of Subdivision Matrices

A given large power network is torn into N subdivisions (1,2,3, $\cdots$ N) by cutting appropriate lines. Subdivision is generally guided by the need to limit the size of each subdivision and is generally performed to separate identifiable power systems, *e.g.*, territories of utilities, provinces, ... , etc. The only restriction on the lines, which should be cut for subdivision, is that no mutual coupling must exist between lines of different subdivisions and between the torn lines.

In addition to a slack bus, selected for the untorn system, a number of temporary buses (TB's) are selected to provided each subdivision with a reference bus (slack or TB). This procedure[5] eliminates singularity and makes all bus admittance matrices well conditioned. For computational simplicity, a temporary bus should not be connected to a line to be cut for subdivision. An N-subdivision system, therefore, has δ ($= N - 1$) temporary buses.

The bus admittance matrix [Y] for each subdivision is constructed in the usual manner using its selected reference (slack or TB) bus. As started earlier, shunt elements to ground including line capacitance are not included in the [Y] matrix.

A shunt admittance vector [YSH] of n_a elements is formed for n_a-bus subdivision where each element is the algebraic sum of the admittances of all shunt elements connected to a bus. There are N vectors of [YSH]: [YSH (1)], [YSH (2)] ..., and [YSH (N)] for N-subdivision system.

An additional diagonal matrix [YTB] of dimensions (δ , δ) is formed for the temporary buses of all subdivisions. An element of [YTB] represents the algebraic sum of the admittances of all lines incident to a temporary bus. By combining the admittance matrices [Y] of all N subdivisions with [YTB], a block diagonal form admittance matrix [Y (bdf)], as shown in Equation (3), of the torn system is obtained.

$$
[\, Y\,(\,bdf\,)] = \begin{array}{c} \\ 1 \\ 2 \\ \\ N \\ \\ \end{array}
\begin{array}{cccc}
1 & 2 & & N \\
Y(1) & & & \\
 & Y(2) & & \\
 & & \ddots & \\
 & & & Y(N) \\
 & & & & YTB
\end{array}
\qquad (3)
$$

The bus admittance matrix [YS] of the whole system is given by

$$[\ YS\ ] = [\ Y_1\ ] + [\ Y_2\ ] \tag{4}$$

where $[\ Y_1\ ] = [\ Y(\ bdf\ )\ I + [\ C\ ]\ [\ Y(\text{ cut })]\ [\ C\ ]^t$ (5)

$[\ Y(\ bdf\ )]$ – is given in Equation (3)

[C] – is a subset of bus connection matrix of dimensions (n , ψ), where ψ number of lines cut for subdivision. It is constructed by inspection and has only + 1 or – 1 for nonzero elements[19]. [Y (cut)] – is a diagonal matrix of dimensions (ψ , ψ) where each element represents the admittance of a cut line, and [Y_2] – is a very sparse matrix containing very few elements corresponding to the buses connected to the temporary buses in the system. Sparsity techniques are used for storing and manipulations of the above matrices.

2.3 Solution Algorithm

Based Eqn (2), the power flow equations of the whole system are given by

$$[\ YS\ ]\ \ [\ E - E_s\ ] = [\ I\ ] \tag{6}$$

Equation (6) can be expressed in the form

$$[\ I\ ] = [\ YS\ ]\ \ [\ \Delta\ E\ ]_{\text{exact}} = [\ Y_1\ ]\ \ [\ \Delta\ E\ ]_{\text{exact}} + [\ Y_2\ ]\ \ [\ \Delta\ E\ ]_{\text{exact}} \tag{7}$$

where [YS] is defined in Eqn (4)

$[\ \Delta\ E\ ]_{\text{exact}}$ is the difference between the required bus voltage (E) and system slack bus voltage (E_s). And [I] is the system bus injected current vector and is calculated by using Eqn (1). Solution of Eqn (6) for $[\ \Delta\ E\ ]_{\text{exact}}$ yields

$$[\ \Delta\ E\ ]_{\text{exact}} = [\ F\ ]^{-1}\ \ [\ \Delta\ E\ ] \tag{8}$$

where
$$[\ \Delta\ E\ ] = [\ Y_1\ ]^{-1}\ \ [\ I\ ] \tag{9}$$

and
$$[\ F\ ] = [\ U\ ] + [\ Y_1\ ]^{-1}\ \ [\ Y_2\ ] \tag{10}$$

In the above equations, [U] is a unity matrix, [$\Delta\ E$] is firstly calculated without actually inverting the matrix [Y_1], and then $[\ \Delta\ E\ ]_{\text{exact}}$ is calculated using [$\Delta\ E$] and the very sparse matrix [F] without explicit matrix inversion. For all above calculations, sparsity techniques are utilized to fullest extent.

Computation of $[\ Y\ ]^{-1}$: The Householder formula[11] gives

$$[\ Y_1\ ]^{-1} = [\ Y(\ bdf\ )]^{-1} - [\ Y(\ bdf\ )]^{-1}\ \ [\ C\ ]\ \ [\ ZC\ ]^{-1}\ \ [\ C\ ]^t\ \ [\ Y(\ bdf\ )]^{-1} \tag{11}$$

where [ZC] (of dimensions ψ , ψ) is defined as the intersubdivision impedance matrix and is given by

$$[\ ZC\ ] = [\ Z(\text{ cut })] + (\ C\ ]^t [\ Y(\ bdf\ )]^{-1}\ \ [\ C\ ] \tag{12}$$

where [Z (cut)] is a diagonal matrix representing the impedances of cut lines. Generally $[\ Y(\ bdf\ )]^{-1}$ is obtained from Eqn (3) either by triangular factorization of subdivision matrices $Y(1)$, $Y(2)$, ... , $Y(N)$ and YTB or by $Z(1)$, $Z(2)$, ... ,

$Z(N)$ and ZTB obtained with respect to its selected reference (slack or TB) bus. In the proposed method, the factorized admittance matrices are used as they always lead to savings in storage and computer time.

Computation of $[\Delta E]$: $[\Delta E]$ is computed from Equations (9) and (11).

$$[\Delta E] = [\Delta E_1] - [\Delta E_2] \tag{13}$$

where $$[\Delta E_1] = [Y(bdf)]^{-1} \; [I] \tag{14}$$

$$[\Delta E_2] = [Y(bdf)]^{-1} \; [C] \; [ZC]^{-1} \; [C]^t \; [\Delta E_1] \tag{15}$$

In the above equations, $[\Delta E_1]$ is a vector of bus voltages differences in the subdivisions and $[\Delta E_2]$ is a vector of corrections in bus voltages differences due to tearing.

2.4 Solution Steps

This section describes the steps for conducting the computations serially by using a single-processor computer.

Step 1 : a) Form and factorize the bus admittance matrix of the first subdivision $[Y(1)]$

b) Compute the subdivision bus injected current vector $[I(1)]$ using Eqn (1). Using $[Y(1)]$ and $[I(1)]$ solve for $[\Delta E_1(1)]$ for subdivision 1 as follows: $[Y(1)][\Delta E_1(1) = [I(1)]$

Repeat step 1 for each subdivision to obtain $[\Delta E_1]$ for the whole system.

Step 2 : Compute $[\Delta EL] = [C]^t [\Delta E_1]$

$[\Delta EL]$ is defined as the changes in cut line voltages with respect to system slack bus.

Step 3 : a) Form $[ZC]$ as defined by Equation (12). It is constructed by using $[Z(\text{cut})]$ and very few elements from very few columns of matrix $[Y]^{-1}$ of each subdivision corresponding to its buses connected to the cut lines.

b) Factorize $[ZC]$

c) Solve $[ZC][\Delta Ic] = [\Delta EL]$ for $[\Delta Ic]$

where $[\Delta Ic]$ are changes in cut line currents.

Step 4 : Calculate $[\Delta I(\text{tie}) = [C][\Delta Ic]$

where $[\Delta I(\text{tie})$ are changes in injected tie currents. For steps 2,3, and 4 no explicit multiplications are required.

Step 5 : Calculate $$[\Delta E_2] = [Y(bdf)]^{-1} [\Delta I(\text{tie})] \tag{16}$$

From Eqn (16), for subdivision 1 we can write

$$[Y(1)][\Delta E_2(1)] = [\Delta I(\text{tie})(1)] \tag{17}$$

Since [Y (1)] is already factorized in step 1, [Δ E_2 (1)] is easily computed without inversion. Similarly, the complete bus correction vector [Δ E_2] is obtained for the whole system by solving Eqn (17) for each subdivision.

Step 6 : Calculate [Δ E] = [Δ E_1] – [Δ E_2]

For temporary buses, [Δ E_1]$_{TB}$ is calculated from

$$[\, \Delta E_1 \,]_{TB} = [\, YTB \,]^{-1} [\, I \,]_{TB} \tag{18}$$

For each subdivision, Δ E_1 of $TB = I_{TB} * ZTB$ where ZTB is the sum of the impedances of all lines incident on to that TB. Since temporary buses are chosen such that they are not connected to cut lines [Δ E_2]$_{TB}$ = 0.

Step 7 : Using Equations (8) and (10), [Δ E]$_{\text{exact}}$ is obtained from [Δ E]

Step 8 : Obtain [E] = [Δ E]$_{\text{exact}}$ + [E_s]

Steps 1 to 8 describe the first iteration. Iterative solution is continued until convergence is obtained according to a chosen tolerance criterion.

2.5 Parallel Solution Scheme

Some of the solution steps described above can proceed in parallel (simultaneously) for all subdivisions (areas) using either a multiprocessor computer or subdivisions single – processor computers in the multicomputer configuration, while the rest must be done sequentially either in the multiprocessor computer or in the central computer of the multicomputer configuration.

An example of multicomputer configuration is shown in Fig. 1, where we have four separate areas (I, II, III, and IV) with a dispatch or related computer in each area plus a central computer (shown in Area I) arranged hierarchially with communication channels linking them.

In this section the solution steps are described for the case of multicomputer configuration. The computers can be physically next to each other thus forming a cluster of computers, or they can be miles apart[4].

The latter case, which is more general, is assumed here, but the results apply to a cluster of computers or to a multiprocessor computer. The procedure for the execution of the parallel solution of the power flow problem using the proposed technique is summarized as follows :

1) Step 1 is executed simultaneously in all area computers to obtain [Δ E_1] for the whole system. Elements of [Δ E_1] corresponding to buses connected to cut lines are sent to the central computer.
2) Steps 2,3, and 4 are executed in the central computer.
3) The currents [Δ I (tie)] obtained from Step 4 are sent back to the subdivision (area) computers.
4) Steps 5, 6, 7 and 8 are conducted in the subdivision computers.

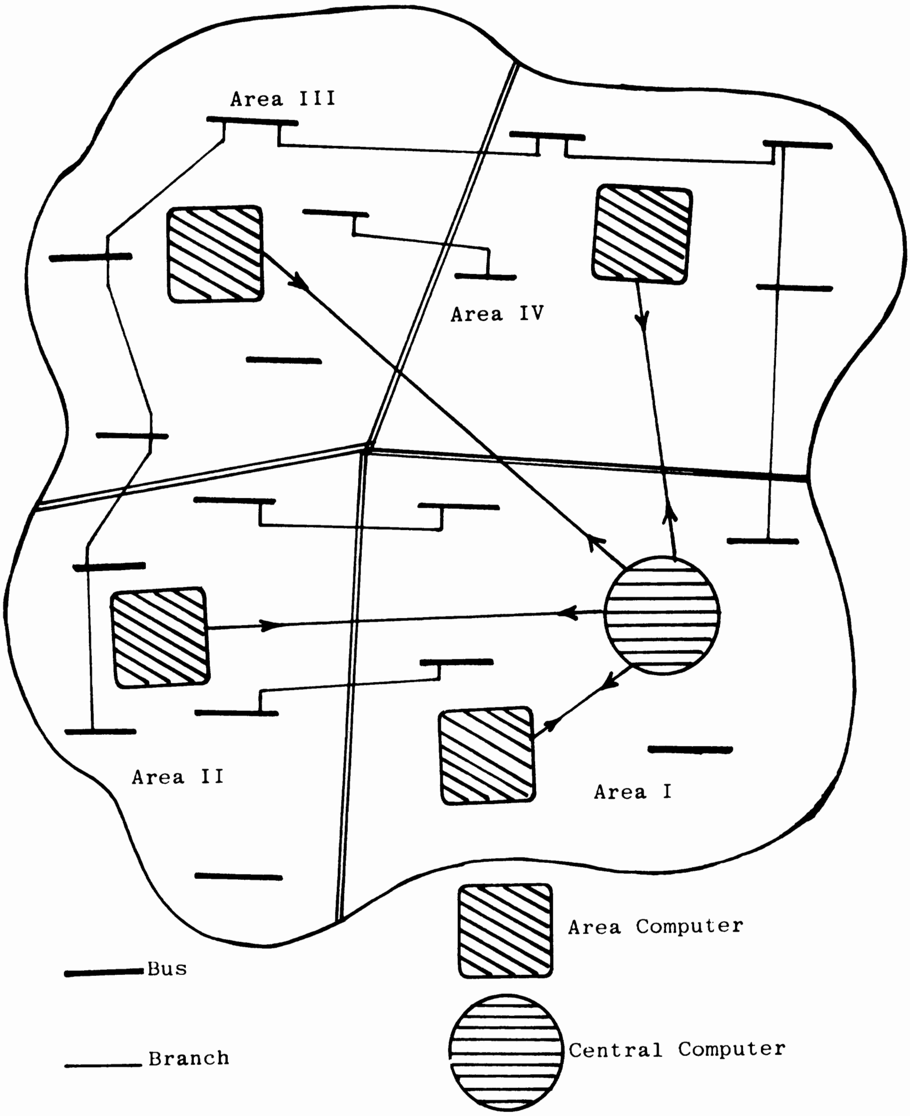

FIG. 1. Multicomputer configuration for four-area power system.

3. Outage Calculations

Compensation methods[15] have been used advantageously for almost any application involving a series of network solutions in which each new case requires modifications in the network matrix with respect to the base case. These methods are based on the inverse-matrix modification technique[16] and employ the already available factors of the base – case network matrix to simulate network changes without re-computing the matrix factors[6,7].

The diakoptical technique proposed for the power flow solution is combined with compensation to simulate the outage of a network element without refactorizing the base – case matrices and starting from the base – case power flow. It determines post contingent network voltages (magnitude and angle) and power flows (active and reactive) in the event of single or multiple – element outages.

Changes in the generation or in the loads can be accommodated in the proposed technique by simply modifying the net bus injected power vectors.

3.1 Single-Branch Outages

Branch (line or transformer) outages are simulated by the application of the inverse – matrix modification technique to the bus admittance matrix of the area in which the outaged branch is located. In the proposed technique the outage of a branch is correctly reflected in both [Y] and [YSH] matrices of the area containing the outaged branch.

If [Y_b] is the base-case matrix and [Y_o] is the outaged-case matrix, then the outage of a branch i, j connecting load buses i and j (in same area) can be simulated in [Y_b] by modifying two elements in row i and two in row j.

$$[\,Y_o\,] = [\,Y_b\,] + [\,M\,]\,[\,\Delta\, y\,]\,[\,M\,]^t \tag{19}$$

where [M] is column vector which is null except for $M_i = a$ and $M_j = -1$. a = off-nominal turns ratio referred to the bus corresponding to row j, for a transformer. a = 1 for a line. [$\Delta\, y$] = – series admittance of line or nominal transformer.

As compared to[6] line charging capacitance and line connected shunt elements of the outaged line are correctly simulated in the outage calculations by removing them from the shunt admittance vector [YSH] corresponding to the buses i and j. Therefore [YSH] is changed in the outaged – case to [YSH_o]. Calculation of [$\Delta\, E_{10}$], vector of [$\Delta\, E_1$] in the outaged – case, is obtained using the outaged – case matrix [Y_o] and the bus – injected current vector [I_o] given by Equation (1) based on the base – case power flow solution and [YSH_o]. For the area containing the outaged branch we have

$$[\,Y_o\,]\,[\,\Delta\, E_{10}\,] = [\,I_o\,] \tag{20}$$

Solution of Eqn (20) is obtained by

$$[\,\Delta\, E_{10}\,] = [\,Y_o\,]^{-1}\,[\,I_o\,] \tag{21}$$

[Y_o]$^{-1}$ is obtained by applying the compensation method to Eqn (19)

$$[\,Y_o\,]^{-1} = [\,Y_b\,]^{-1} - [\,Y_b\,]^{-1}[\,M\,][\,C_1\,][\,M\,]^t[\,Y_b\,]^{-1} \tag{22}$$

where

$$[\,C_1\,] = [\,[\,\Delta\, y\,]^{-1} + [\,M\,]^t[\,Y_b\,]^{-1}[\,M\,]\,]^{-1} \tag{23}$$

C_1 is scalar for single-outage cases

Substitution of Eqn (22) into Eqn (21), we have

$$[\,\Delta E_{10}\,] = [\,Y_o\,]^{-1}[\,I_o\,]$$
$$= [\,\Delta E_{1b}\,] - [\,Y_b\,]^{-1}[\,M\,][\,C_1\,][\,M\,]^t[\,\Delta E_{1b}\,] \qquad (24)$$

where $[\,\Delta E_{1b}\,] = [\,Y_b\,]^{-1}[\,I_o\,]$ (25)

$[\,\Delta E_{1b}\,]$ is calculated using the already available factorized base – case matrix and the base – case bus injected current vector modified at buses i and j to reflect modifications in [YSH]. It should be stated that no explicit matrix multiplications are needed in Eqn (24) and sparsity is fully exploited.

3.2 Multiple-Branch Outages

When a number (m) of branches are outaged simultaneously, [Δy] shown in Eqn (19) becomes a diagonal matrix of size (m, m) where an element represents the series admittance of an outaged branch, and [M] becomes a matrix of m columns, each with entries + 1 (or a) and – 1 in the relevant positions. [C_1] in this case is a (m, m) matrix. Also [YSH] should be modified to correctly reflect the removal of shunt elements associated with the outaged branches.

3.3 Cut-Line Outages

If a line selected for cut for subdivision is outaged, then this outage should be simulated by modifying the following matrices: [C], [Y (cut)] and [ZC]. Entries of the column of [C] corresponding to the outaged cut-line are zeros and so are elements of [Y (cut)] and [ZC]. Also shunt-element admittances are correctly removed from [YSH] vectors of the two areas interconnected by the cut-line.

3.4 Solution Steps and Parallel Solution

Same solution steps and parallel processing solution scheme described in the last section are followed for the outage studies provided that proper modifications must be done as just stated for simulating different outaged cases.

4. Results

4.1 Power Flow Solution of a Sample System

The proposed diakoptical technique has been applied to provide power flow solution of a number of power systems. As an example of IEEE-14 bus test system is solved to demonstrate the effectiveness of the proposed solution technique. The test system, shown in Fig. 2, is divided into two areas A and B by cutting 5 lines. Bus 7 in area A is the system slack bus and bus 7 is selected as the temporary bus of area B. Data of IEEE-14 bus system is known and is given in Reference [20].

Table 1 provides the results obtained by applying the proposed technique. These results are exactly the same and show the same convergence when the untorn system is solved as a whole.

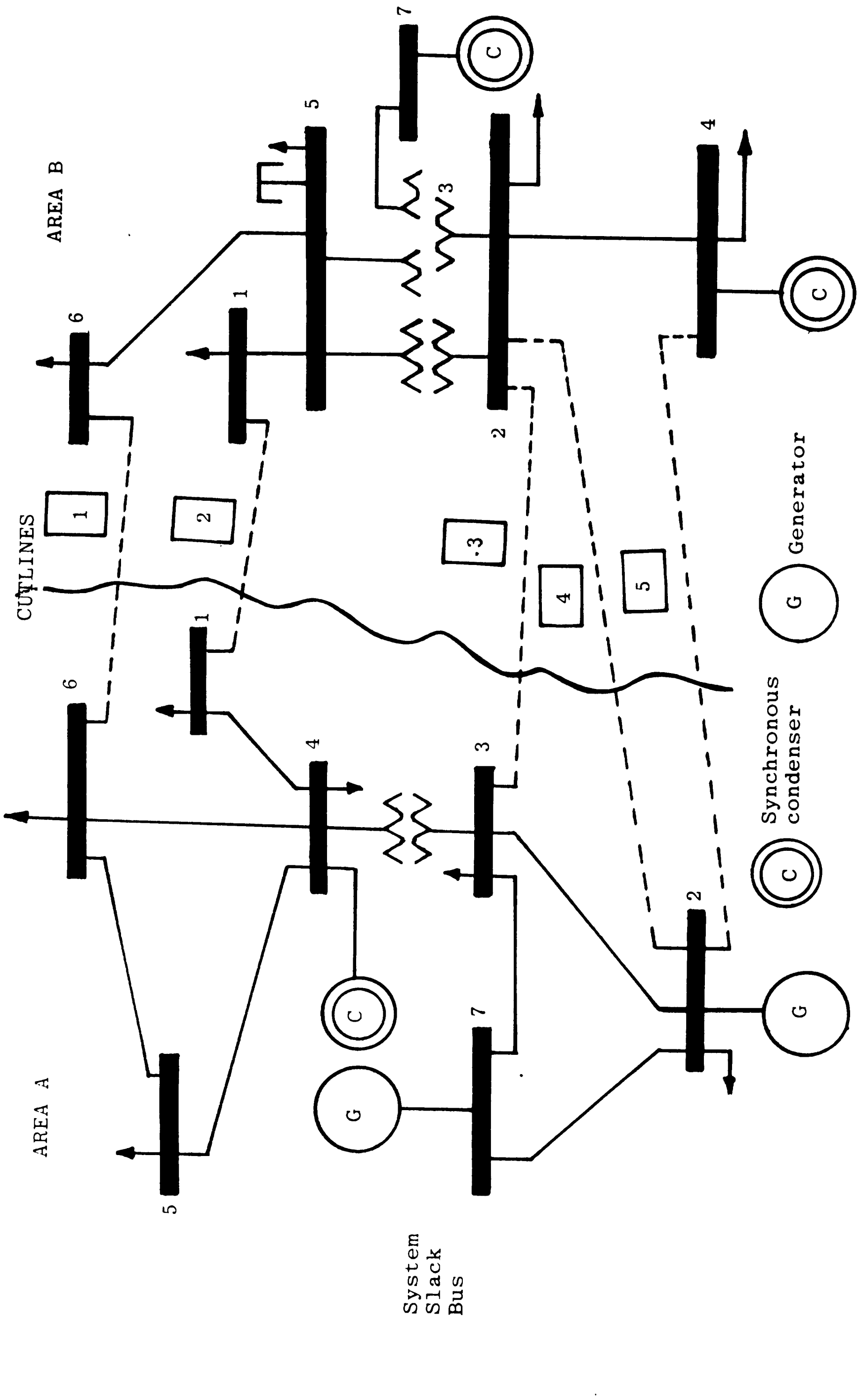

FIG. 2. IEEE-14 bus test system.

TABLE 1. Calculated active and reactive line flows and bus voltages for IEEE – 14-bus system in the base case.

Area	Line no.	From bus	To bus	Line power flow: Active MW	Line power flow: Reactive MVARS	Bus no. & area	Bus voltage: Magnitude V(PU)	Bus voltage: Angle (Degrees)
A	1	2	7	165.10	10.89	1 A	1.055	- 15.15
A	2	3	7	76.63	- 5.69	2 A	1.026	- 5.01
A	3	2	3	36.59	- 20.49	3 A	1.040	- 9.00
A	4	3	4	41.85	- 2.14	4 A	1.050	- 14.55
A	5	4	5	5.54	- 1.90	5 A	1.048	- 15.41
A	6	4	6	13.02	- 2.07	6 A	1.045	- 15.50
A	7	1	4	3.75	- 4.49	7 A	1.050	0.00
A	8	5	6	1.40	0.42	1 B	1.055	- 15.48
						2 B	1.038	- 10.54
B	1	2	3	29.43	- 18.49	3 B	1.077	- 13.70
B	2	2	5	16.52	- 3.97	4 B	1.010	- 12.78
B	3	4	2	26.64	4.94	5 B	1.063	- 15.32
B	4	3	5	29.45	14.03	6 B	1.037	- 16.40
B	5	3	7	0.01	- 15.81	7 B	1.050	- 13.70
B	6	5	6	10.23	5.41			
B	7	5	1	6.26	7.04			
Cut Lines	1	6 A	6 B	4.85	- 0.03			
	2	1 A	1 B	2.77	- 1.16			
	3	3 A	2 B	64.25	- 14.53			
	4	2 A	2 B	51.27	- 22.83			
	5	2 A	4 B	69.92	- 5.81			

The results presented in Table 1 are obtained in 5 iterations starting from the flat voltage start by using single-processor computer for sequentially solving the torn system. However, using a multiple-processor computer or a group of single-processor computers will provide exactly the same results but with lesser computation time and higher speed.

4.2 Outage Studies

Test results are presented in this section to demonstrate the effectiveness of the proposed diakoptical technique for outage (contingency) studies. The IEEE-14 bus system described above is used.

Three study cases were run: One representing an outage of a heavily loaded line (line no. 2 that was carrying 76.63 MW in the preoutage state), the second is an outage of line no. 3 which represents a medium loading case (36.59 MW in the base case) and the third represents an outage of lightly loaded line (line no. 6 that was carrying 13.02 MW in the preoutage state). Tables 2, 3, and 4 provide calculated active and reactive line flows obtained by using the proposed technique for a single outage of lines number 2, 3 and 6 respectively. For comparison, a full power flow solution is also obtained in which the outage is simulated by physically removing the line. Full solution was provided by using both Gauss-Jacobi Z-bus method of the whole (untorn) system and the proposed diakoptical technique for power flow. Once again, the results of the full solution of outaged lines by both methods are exactly the same. Results of the full solution and the difference (between the full and proposed technique solutions) in calculated active and reactive line flows are also provided in Tables 2,3, and 4.

TABLE 2. Comparison of calculated active and reactive line flows for IEEE-14-bus system with outage of line no. 2 (76.63 M W, – 5.69 M V A R).

Area	Line no.	MW flows		MVAR flows		Difference	
		Full	Proposed	Full	Proposed	MW	MVAR
A	1	236.59	236.59	– 4.20	– 4.20	0.0	0.0
A	2	0.0	0.0	0.0	0.0	0.0	0.0
A	3	78.34	78.34	– 5.00	– 5.01	0.0	0.01
A	4	41.10	41.10	– 18.90	– 18.89	0.0	– 0.01
A	5	12.99	12.99	13.42	13.41	0.0	0.01
A	6	27.89	27.88	27.46	27.46	0.01	0.0
A	7	12.03	12.03	15.40	15.40	0.0	0.0
A	8	1.25	1.25	0.49	0.49	0.0	0.0
B	1	30.78	30.78	– 16.28	– 16.28	0.0	0.0
B	2	17.26	17.26	– 2.97	– 2.97	0.0	0.0
B	3	6.32	6.32	– 11.66	– 11.66	0.0	0.0
B	4	30.79	30.79	14.63	14.63	0.0	0.0
B	5	0.01	0.01	10.02	10.01	0.0	0.01
B	6	11.05	11.04	5.20	5.20	0.01	0.0
B	7	7.52	7.52	6.68	6.68	0.0	0.0
Cut Lines	1	4.06	4.06	0.24	0.24	0.0	0.0
	2	1.51	1.51	– 0.79	– 0.79	0.0	0.0
	3	26.93	26.93	– 8.90	– 8.90	0.0	0.0
	4	84.00	84.00	– 6.47	– 6.48	0.0	0.01
	5	84.97	84.96	– 7.05	– 7.05	0.01	0.0

Full = Full power flow solution.
Proposed = Proposed outages technique.

The proposed technique has been found to give very accurate results in computing bus voltages in the outaged state as shown from Table 5 which provides comparison of calculated bus voltages magnitudes for the test system with the three single-outage cases defined above.

Also the proposed technique gives very good accuracy in computing post-contingency active and reactive power flows.

Table 6 lists the magnitude of the maximum and average relative errors in line active and reactive power flows and in bus voltage magnitudes. It is shown that the maximum relative error for active line flows is 0.09%, 0.12% and 0.0% for the three cases of high, medium and light loading respectively. The corresponding average

TABLE 3. Comparison of calculated active and reactive line flows for IEEE-14-bus system with outage of line no. 3 (36.59 M W, – 20.49 M V A R).

Area	Line no.	MW flows		MVAR flows		Difference	
		Full	Proposed	Full	Proposed	MW	MVAR
A	1	149.58	149.57	14.59	14.59	0.01	0.0
A	2	92.20	92.19	- 2.93	- 2.95	0.01	0.02
A	3	0.0	0.0	0.0	0.0	0.0	0.0
A	4	40.65	40.64	- 5.53	- 5.52	0.01	- 0.01
A	5	6.91	6.90	1.10	1.09	0.01	0.01
A	6	15.58	15.56	3.71	3.68	0.02	0.03
A	7	4.72	4.71	- 0.53	- 0.55	0.01	0.02
A	8	1.29	1.29	0.46	0.46	0.0	0.0
B	1	30.38	30.38	- 18.09	- 18.10	0.0	0.01
B	2	17.05	17.05	- 3.79	- 3.80	0.0	0.1
B	3	17.18	17.19	3.81	3.82	- 0.01	- 0.01
B	4	30.39	30.39	14.05	14.05	0.0	0.0
B	5	0.01	0.01	- 11.17	- 11.20	0.0	0.03
B	6	10.80	10.80	5.30	5.29	0.0	0.01
B	7	7.15	7.15	6.85	6.85	0.0	0.0
Cut Lines	1	4.29	4.29	0.11	0.11	0.0	0.0
	2	1.88	1.88	- 0.97	- 0.98	0.0	0.01
	3	39.74	39.74	9.16	- 9.16	0.0	0.0
	4	69.59	69.58	- 22.49	- 22.51	0.01	0.02
	5	78.41	78.41	- 6.56	- 6.56	0.0	0.0

error is 0.007%, 0.025% and 0.0% respectively.

The maximum error for reactive line flows is 0.20%, 3.77%, and 0.28% for the three cases of loading respectively and the corresponding average error is 0.029%, 0.439% and 0.017% respectively. It should be noted that the highest error (3.77%) occurs for a line with little reactive power flow, which minimizes the significance of the relative error.

The proposed technique can be applied for both single and multiple outages. However, in order to limit the length of the paper, we have provided only the results of single-outage cases.

All the tests presented in this paper were performed with a tolerance of 0.001 per unit for both the real and imaginary components of bus voltages. The number of iterations required for convergence ranged from 1 to 6 depending on the outaged branch being simulated. However, the majority of cases required only 1 to 2 iterations. Compared with the full power flow solution using the proposed diakoptical technique, the proposed technique for outage studies has a computation time advantage of 1 to 2.

5. Conclusion

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TABLE 4. Comparison of calculated active and reactive line flows for IEEE-14-bus system with outage of line no. 6 (13.02 M W, – 2.07 M V A R).

Area	Line no.	MW flows		MVAR flows		Difference	
		Full	Proposed	Full	Proposed	MW	MVAR
A	1	165.34	165.34	10.84	10.84	0.0	0.0
A	2	76.73	76.73	– 5.05	– 5.05	0.0	0.0
A	3	36.76	36.76	– 19.73	– 19.73	0.0	0.0
A	4	39.56	39.56	– 2.92	– 2.92	0.0	0.0
A	5	16.51	16.51	0.58	0.58	0.0	0.0
A	6	0.0	0.0	0.0	0.0	0.0	0.0
A	7	6.63	6.63	– 4.33	– 4.33	0.0	0.0
A	8	12.54	12.54	2.95	2.95	0.0	0.0
B	1	31.38	31.38	– 16.18	– 16.18	0.0	0.0
B	2	17.62	17.62	– 2.67	– 2.67	0.0	0.0
B	3	25.94	25.94	3.53	3.51	0.0	– 0.01
B	4	31.40	31.40	16.02	16.01	0.0	0.01
B	5	0.02	0.02	– 11.63	– 11.63	0.0	0.0
B	6	16.62	16.62	9.04	9.04	0.0	0.0
B	7	2.92	2.92	6.01	6.01	0.0	0.0
Cut Lines	1	1.32	1.32	3.19	3.19	0.0	0.0
	2	6.12	6.12	– 0.12	– 0.12	0.0	0.0
	3	66.53	66.53	– 11.99	– 11.99	0.0	0.0
	4	51.96	51.96	– 21.45	– 21.45	0.0	0.0
	5	70.18	70.18	– 5.83	– 5.83	0.0	0.0

TABLE 5. Comparison of calculated bus voltage magnitudes for IEEE-14-bus system with the 3 single-outage cases (per unit).

Area	Bus no.	Outage of line no. 2			Outage of line no. 3			Outage of line no. 6		
		Full	Proposed	Difference	Full	Proposed	Difference	Full	Proposed	Difference
A	1	1.010	1.010	0.0	1.047	1.047	0.0	1.052	1.052	0.0
A	2	1.026	1.026	0.0	1.026	1.026	0.0	1.026	1.026	0.0
A	3	0.997	0.997	0.0	1.032	1.032	0.0	1.039	1.039	0.0
A	4	1.050	1.050	0.0	1.050	1.050	0.0	1.050	1.050	0.0
A	5	1.002	1.002	0.0	1.039	1.039	0.0	1.030	1.030	0.0
A	6	0.999	0.999	0.0	1.036	1.036	0.0	0.998	0.998	0.0
B	1	1.010	1.010	0.0	1.047	1.047	0.0	1.048	1.048	0.0
B	2	0.997	0.997	0.0	1.030	1.030	0.0	1.035	1.035	0.0
B	3	1.033	1.033	0.0	1.069	1.069	0.0	1.070	1.070	0.0
B	4	1.010	1.010	0.0	1.010	1.010	0.0	1.010	1.010	0.0
B	5	1.018	1.018	0.0	1.055	1.055	0.0	1.054	1.054	0.0
B	6	0.991	0.991	0.0	1.028	1.028	0.0	1.011	1.011	0.0
B	7	1.050	1.050	0.0	1.050	1.050	0.0	1.050	1.050	0.0

TABLE 6. Percent maximum and average error in line flows and bus voltage magnitudes for IEEE-14-bus system with the 3 single-outage cases.

Error in % →	MW flows		MVAR flows		Voltage	
Outaged line Line no. ↓	Max.	Ave.	Max.	Ave.	Max.	Ave.
2	0.09	0.007	0.20	0.029	0.0	0.0
3	0.12	0.025	3.77*	0.439	0.0	0.0
6	0.0	0.0	0.28	0.17	0.0	0.0

*Occurs for a line with little power flow, which minimizes the significance of this relative error.

size power systems has been presented. The proposed technique has the following attractive features :

1) The solution technique is exact and hence produces the same power flow solution and has the same convergence property of the original untorn system.

2) The singularity of bus matrices is avoided and instead they are well-conditioned by selecting a temporary bus as reference in each subdivision except the one containing the system slack bus.

3) The technique does not impose any restriction on the impedance of lines to be cut for tearing.

4) The technique combine both diakoptics and compensation methods for simulating branch outages without reconstructing or refactorizing the system matrices of the precontingency state. It has been shown that the results obtained are very accurate as compared to the full power flow solution of outage problems.

5) The proposed technique can either be used in a single-processor computer for sequential solution of torn areas or in multi-computer configuration for a faster solution by parallel processing of torn areas.

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حـــل مســائــل ســريان الـقـــدرة والــطــواريء باسـتـخـــدام الحــل بالتقطيـــع والتعـــويض

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المستخلص . يصف البحث طريقة داياكوبتيكية (الحل بالتقطيع) لحل مسائل سريان القدرة لنظم القوى الكهربائية ذات الحجم الكبير جدًا ، وتجمع طريقتي الحل بالتقطيع والتعـويض لتمثيل وحـل مسـائـل طواريء (خروج) الفروع بدون إعادة بناء أو تحليل مصفوفات نظم القوى الخاصة بحالة ماقبل الطواريء . ويمكن استخدام الطرق المقترحة في هذا البحث في حاسب آلي (كمبيوتر) ذي معالج واحد ، وذلك بالحل التتابعي للأقسام المقطعة أو استخدامها في الحل المتوازي (لكل الأقسام في نفس الوقت) عن طريق استخدام كمبيوتر متعدد المعالجات للحصول على حل أسرع .

تعطي الطريقة المقترحة نفس نتائج النظام الكبير (الواحد) لو تم حله ودراسته بدون تقطيع .

وتعطي الطريقة الجديدة نتائج حل مسائل الطواريء متمثلة في مقدار وزاوية الجهد وسريان القدرة الفعالة وغير الفعالة في دراسات الطواريء سواءً كانت أحادية أو متعددة ، وذلك في وقت أقل بالمقارنة لحل الطواريء باستخدام الحل الكامل لسريان القدرة .

ويحتوي البحث على وسائل تطبيق الطريقة المقترحة في الحل التتابعي والحل المتوازي ونتائج تطبيقها على عينة نظام .